



BOX 1 OF 2 PCT  
JC10 Rec'd PCT/PTO 13 MAY 2005

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

<b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>		Docket Number: 02885/93	
Application Number 10/523,764	Filing Date February 7, 2005	Examiner to be assigned	Art Unit to be assigned
Invention Title <b>DATA PROCESSING METHOD AND DEVICE</b>		Inventor(s) Martin VORBACH et al.	

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

Date: 10 May 2005 Reg. No. 36,098

Signature: Michelle Carniaux

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant(s) hereby bring the following reference(s) to the attention of the Examiner. The reference(s) are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b).
2. A copy of each patent, publication or other information listed on the modified PTO form 1449 is enclosed, except as otherwise indicated on the modified PTO form 1449.
3. The Commissioner is hereby authorized to charge payment of the 37 C.F.R. §1.17(p) (submission of an information disclosure statement under §1.97(c)) fee of **\$180.00** and any additional fees that may be required to the deposit account of Kenyon & Kenyon, deposit account number **11-0600**.

Dated: 10 May 2005

By:

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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT  
PTO FORM 1449

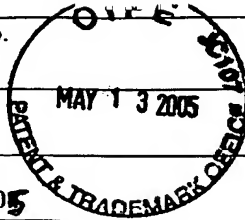
Atty. Docket No.  
02885/93

Applicant(s)  
Vorbach et al.

Filing Date  
February 7, 2005

Serial No.  
10/523,764

Group Art Unit  
to be assigned



**\*U. S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLAS S	SUB CLASS	FILING DATE
	RE34363	August 31, 1993	Freeman			
	2,067,477	January 12, 1937	J.B. Cooper			
	3,242,998	March 29, 1966	C.H. Gubbins			
	3,681,578	August 1, 1972	Stevens			
	3,757,608	September 11, 1973	Willner			
	3,855,577	December 17, 1974	Vandierendonck			
	4,489,857	February 6, 1996	Agrawal et al.			
	4,498,134	February 5, 1985	Etchells et al.			
	4,498,172	February 5, 1985	Bhavsar			
	4,566,102	January 21, 1986	Hefner			
	4,591,979	May 27, 1986	Iwashita			
	4,663,706	May 5, 1987	James et al.			
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	4,739,474	April 19, 1988	Holsztynski			
	4,761,755	August 2, 1988	Ardini et al.			
	4,811,214	March 7, 1989	Nosenchuck et al.			
	4,852,043	July 25, 1989	Guest			
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	4,860,201	August 22, 1989	Miranker et al.			
	4,870,302	September 26, 1989	Freeman			
	4,891,810	January 2, 1990	de Corlieu et al.			
	4,901,268	February 13, 1990	Judd			
	4,910,665	March 20, 1990	Matheyses et al.			
	4,967,340	October 30, 1990	Dawes			
	5,014,193	May 7, 1991	Garner et al.			
	5,015,884	May 14, 1991	Agrawal et al.			
	5,021,947	June 4, 1991	Campbell et al.			
	5,023,775	June 11, 1991	Poret			
	5,043,978	August 27, 1991	Nagler et al.			
	5,047,924	September 10, 1991	Matsubara et al.			
	5,065,308	November 12, 1999	Evans			
	5,072,178	December 10, 1991	Matsumoto			
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	5,109,503	April 28, 1992	Cruickshank et al.			
	5,113,498	May 12, 1992	Evan et al.			

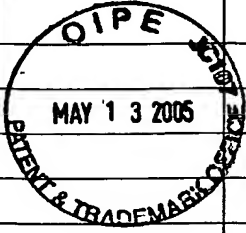
EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLAS S	SUB CLASS	FILING DATE
	5,113,498	May 12, 1992	Evan et al.			
	5,115,510	May 19, 1992	Okamoto et al.			
	5,123,109	June 16, 1992	Hillis			
	5,125,801	June 30, 1992	Nabity et al.			
	5,128,559	July 7, 1992	Steele			
	5,142,469	August 25, 1992	Weisenborn			
	5,144,166	September 1, 1992	Camarota et al.			
	5,193,202	March 9, 1993	Lee et al.			
	5,203,005	April 13, 1993	Horst			
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	5,208,491	May 4, 1993	Ebeling et al.			
	5,226,122	July 6, 1993	Thayer et al.			
	5,233,539	August 3, 1993	Agrawal et al.			
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	5,274,593	December 28, 1993	Proebsting			
	5,287,472	February 15, 1994	Horst			
	5,294,119	March 15, 1994	Vincent et al.			
	5,301,284	April 5, 1994	Estes et al.			
	5,301,344	April 5, 1994	Kolchinsky			
	5,303,172	April 12, 1994	Magar et al.			
	5,336,950	August 9, 1994	Popli et al.			
	5,347,639	September 13, 1994	Rechtschaffen et al.			
	5,349,193	September 20, 1994	Mott et al.			
	5,353,432	October 4, 1994	Richek et al.			
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	5,379,444	January 3, 1995	Mumme			
	5,410,723	April 25, 1995	Schmidt et al.			
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	5,422,823	June 6, 1995	Agrawal et al.			
	5,425,036	June 13, 1995	Liu et al.			
	5,426,378	June 20, 1995	Ong			
	5,428,526	June 27, 1995	Flood et al.			
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	5,440,245	August 8, 1995	Galbraith et al.			
	5,440,538	August 15, 1995	Olsen et al.			
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	5,444,394	August 22, 1995	Watson et al.			
	5,448,186	September 5, 1995	Kawata			
	5,455,525	October 3, 1995	Ho et al.			
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		5,473,267	December 5, 1995	Stansfield			
		5,475,583	December 12, 1995	Bock et al.			
		5,475,803	December 12, 1995	Stearns et al.			
		5,475,856	December 12, 1995	Kogge			
		5,483,620	January 9, 1996	Pechanek et al.			
		5,485,103	January 16, 1996	Pedersen et al.			
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		5,489,857	February 6, 1996	Agrawal et al.			
		5,491,353	February 13, 1996	Kean			
		5,493,239	February 20, 1996	Zlotnick			
		5,497,498	March 5, 1996	Taylor			
		5,506,998	April 9, 1996	Kato et al.			
		5,510,730	April 23, 1996	El Gamal et al.			
		5,511,173	April 23, 1996	Yamaura et al.			
		5,513,366	April 30, 1996	Agarwal et al.			
		5,521,837	May 28, 1996	Frankle et al.			
		5,522,083	May 28, 1996	Gove et al.			
		5,530,873	June 25, 1996	Takano			
		5,530,946	June 25, 1996	Bouvier et al.			
		5,532,693	July 2, 1996	Winters et al.			
		5,532,957	July 2, 1996	Malhi			
		5,535,406	July 9, 1996	Kolchinsky			
		5,537,057	July 16, 1996	Leong et al.			
		5,537,601	July 16, 1996	Kimura et al.			
		5,541,530	July 30, 1996	Cliff et al.			
		5,544,336	August 6, 1996	Kato et al.			
		5,548,773	August 20, 1996	Kemeny et al.			
		5,555,434	September 10, 1996	Carlstedt			
		5,559,450	September 24, 1996	Ngai et al.			
		5,561,738	October 1, 1996	Kinerk et al.			
		5,570,040	October 29, 1996	Lytle et al.			
		5,574,930	November 12, 1996	Halverson Jr. et al.			
		5,583,450	December 10, 1996	Trimberger et al.			
		5,586,044	December 17, 1996	Agrawal et al.			
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		5,590,345	December 31, 1996	Barker et al.			
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		5,600,265	February 4, 1997	El Gamal Abbas et al.			

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	5,600,845	February 4, 1997	Gilson			
	5,611,049	March 11, 1997	Pitts			
	5,617,547	April 1, 1997	Feeney et al.			
	5,625,806	April 29, 1997	Kromer			
	5,634,131	May 27, 1997	Matter et al.			
	5,649,176	July 15, 1997	Selvidge et al.			
	5,649,179	July 15, 1997	Steenstra et al.			
	5,652,894	July 29, 1997	Hu et al.			
	5,655,069	August 5, 1997	Ogawara et al.			
	5,655,124	August 5, 1997	Lin			
	5,657,330	August 12, 1997	Matsumoto			
	5,658,797	August 19, 1997	Zandveld et al.			
	5,675,743	October 7, 1997	Mavity			
	5,680,583	October 21, 1997	Kuijsten			
	5,713,037	January 27, 1998	Wilkinson et al.			
	5,717,943	February 10, 1998	Barker et al.			
	5,732,209	March 24, 1998	Vigil et al.			
	5,734,921	March 31, 1998	Dapp et al.			
	5,742,180	April 21, 1998	Detton et al.			
	5,748,872	May 5, 1998	Norman			
	5,754,827	May 19, 1998	Barbier et al.			
	5,754,871	May 19, 1998	Wilkinson et al.			
	5,760,602	June 2, 1998	Tan			
	5,761,484	June 2, 1998	Agarwal et al.			
	5,773,994	June 30, 1998	Jones			
	5,778,439	July 7, 1998	Timberger et al.			
	5,784,636	July 21, 1998	Rupp			
	5,794,059	August 11, 1998	Barker et al.			
	5,794,062	August 11, 1998	Baxter			
	5,801,715	September 1, 1998	Norman			
	5,802,290	September 1, 1998	Casselman			
	5,828,229	October 27, 1998	Cliff et al.			
	5,828,858	October 27, 1998	Athanas et al.			
	5,838,165	November 17, 1998	Chatter			
	5,844,888	December 1, 1998	Narjyka			
	5,848,238	December 8, 1998	Shimomura et al.			
	5,854,918	December 29, 1998	Baxter			
	5,859,544	January 12, 1999	Norman			
	5,865,239	February 2, 1999	Carr			
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	5,901,279	May 4, 1999	Davis III			
	5,915,123	June 22, 1999	Mirsky et al.			
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	5,978,260	November 2, 1999	Trimberger et al.			
	6,011,407	January 4, 2000	New			
	6,014,509	January 11, 2000	Furtek et al.			
	6,020,758	February 1, 2000	Patel et al.			
	6,021,490	February 1, 2000	Vorbach et al.			
	6,023,564	February 8, 2000	Trimberger			
	6,023,742	February 8, 2000	Ebeling et al.			
	6,034,538	March 7, 2000	Abramovici			
	6,038,650	March 14, 2000	Vorbach et al.			
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	6,047,115	April 4, 2000	Mohan et al.			
	6,049,222	April 11, 2000	Lawman			
	6,052,773	April 18, 2000	DeHon et al.			
	6,054,873	April 25, 2000	Laramie			
	6,058,469	May 2, 2000	Baxter			
	6,081,903	June 27, 2000	Vorbach et al.			
	6,085,317	July 4, 2000	Smith			
	6,086,628	July 11, 2000	Dave et al.			
	6,088,795	July 11, 2000	Vorbach et al.			
	6,092,174	July 18, 2000	Roussakov			
	6,105,105	August 15, 2000	Trimberger et al.			
	6,108,760	August 22, 2000	Mirsky et al.			
	6,119,181	September 12, 2000	Vorbach et al.			
	6,122,719	September 19, 2000	Mirsky et al.			
	6,125,408	September 26, 2000	McGee et al.			
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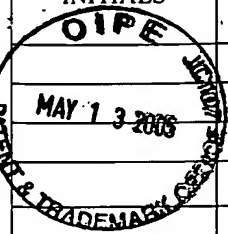
EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLAS S	SUB CLASS	FILING DATE
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	6,173,434	January 9, 2001	Wirthlin et al.			
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	6,219,833	April 17, 2001	Solomon et al.			
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	6,240,502	May 29, 2001	Panwar et al.			
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	6,260,179	July 10, 2001	Ohsawa et al.			
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	6,289,440	September 11, 2001	Casselman			
	6,298,472	October 2, 2001	Phillips et al.			
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	6,338,106	January 8, 2002	Vorbach et al.			
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	6,347,346	February 12, 2002	Taylor			
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	6,370,596	April 9, 2002	Dakhil			
	6,378,068	April 23, 2002	Foster et al.			
	6,389,379	May 14, 2002	Lin et al.			
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	6,538,468	March 25, 2003	Moore			
	6,539,477	March 25, 2003	Seawright			

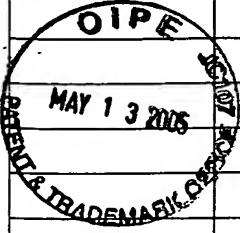
EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/ PUBLICATION DATE	NAME	CLAS S	SUB CLASS	FILING DATE
	6,542,998	April 1, 2003	Vorbach et al.			
	6,571,381	May 27, 2003	Vorbach et al.			
	6,587,939	July 1, 2003	Takano			
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	6,687,788	February 3, 2004	Vorbach et al.			
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	6,717,436	April 6, 2004	Kress et al.			
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	2003/0056202	March 20, 2003	Vorbach			
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\*Copies of the U.S. Patent and U.S. Publication References are not provided pursuant to Official Gazette notice dated August 5, 2003.



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EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO
	0 208 457	June 24, 1986	Europe				
	0 221 360	May 13, 1987	Europe				
	0 428 327	May 22, 1991	Europe				
	0 463 721	January 2, 1992	Europe				
	0 477 809	April 1, 1992	Europe				
	0 485 690	May 20, 1992	Europe				
	0 497 029	August 5, 1992	Europe				
	0 539 595	May 5, 1993	Europe				
	0 628 917	December 14, 1994	Europe				
	0 678 985	October 25 1995	Europe				
	0 686 915	December 13, 1995	Europe				
	0 707 269	April 17 1996	Europe				
	0 726 532	July 2, 1998	Europe				
	0 735 685	October 2, 1996	Europe				
	0 748 051	December 11, 1996	Europe				
	0 835 685	October 2, 1996	Europe				
	0 926 594	June 30, 1999	Europe				
	1 102 674	July 13, 1999	Europe				
	1 146 432	October 17, 2001	Europe				
	2 752 466	February 20, 1998	France				
	38 55 673	November 20, 1996	Germany				
	42 21 278	January 5, 1994	Germany				
	44 16 881	November 17, 1994	Germany				
	100 28 397	December 20, 2001	Germany				
	100 36 627	February 14, 2002	Germany				
	101 29 237	April 18, 2002	Germany				
	102 04 044	August 14, 2003	Germany				
	196 51 075	June 10, 1998	Germany				
	196 54 593	July 2, 1998	Germany				
	196 54 595	July 2, 1998	Germany				
	196 54 846	July 9, 1998	Germany				
	197 04 044	August 13, 1998	Germany				
	197 04 728	August 13, 1998	Germany				
	197 04 742	September 24, 1998	Germany				
	198 07 872	August 26, 1999	Germany				
	198 61 088	February 10, 2000	Germany				

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO
	199 26 538	December 14, 2000	Germany				
	WO90/04835	May 3, 1990	PCT				
	WO90/11648	October 4, 1990	PCT				
	WO93/11503	June 10, 1993	PCT				
	WO94/08399	April 14, 1994	PCT				
	WO94/06077	March 17, 1994	PCT				
	WO95/00161	January 5, 1995	PCT				
	WO95/26001	September 28, 1995	PCT				
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	WO02/29600	April 11, 2002	PCT				
	WO02/71248	September 12, 2002	PCT				
	WO02/71249	September 12, 2002	PCT				
	WO02/103532	December 27, 2002	PCT				
	WO03/17095	February 27, 2003	PCT				
	WO03/23616	March 30, 2003	PCT				
	WO03/25781	March 27, 2003	PCT				
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	WO03/36507	May 1, 2003	PCT				

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